REMARKS

In the non-final Office Action, the Examiner rejects claim 1 under 35 U.S.C. § 102(b) as anticipated by SMITH et al. (U.S. Patent No. 5,579,341) in view of KIM (U.S. Patent No. 6,459,679); rejects claims 27 and 28 under 35 U.S.C. § 102(e) as anticipated by BEAMISH et al. (U.S. Patent No. 6,445,732); rejects claim 29 under 35 U.S.C. § 103(a) as unpatentable over BEAMISH et al. in view of O'DONNELL et al. (U.S. Patent No. 4,983,970); and allows claims 2-26.

By way of the present amendment, Applicant amends claim 1 to improve form. No new matter has been added by way of the present amendment. Claims 1-29 remain pending.

Applicant notes with appreciation the indication that claims 2-26 are allowed over the art of record. Applicant respectfully traverses the rejections of claims 1 and 27-29 under 35 U.S.C. §§ 102 and 103.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as allegedly anticipated by SMITH et al. in view of KIM. Applicant respectfully traverses this rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. See M.P.E.P. § 2131. SMITH et al. and KIM do not disclose or suggest the combination of features recited in claim 1, as currently amended.

Amended independent claim 1 is directed to a method of operating a digital tuner. The method includes amplifying a first number of input signals via a variable gain

amplifier, where an amplifier gain of the variable gain amplifier is set as a function of an entire carrier multiplex present on the first number of input signals; digitizing the amplified first number of input signals to create respective streams of digitized input data; providing a second number of per-channel front-ends for performing baseband translation and filtering in the digital domain and providing outputs suitable for subsequent demodulation; providing each per-channel front-end with an input selector coupled to each of the streams of digitized input data; and configuring each of the per-channel front-ends to process a selected one of the first number of streams of digitized input data. SMITH et al. and KIM do not disclose or suggest this combination of features.

For example, SMITH et al. and KIM do not disclose or suggest amplifying a first number of input signals via a variable gain amplifier, where an amplifier gain is set as a function of an entire carrier multiplex present on the first number of input signals. In stark contrast, SMITH et al. discloses received input signals being mixed at a mixer 204 and then digitized via A/D converters 10 (see Fig. 2). SMITH et al. in no way discloses or suggests that mixer 204 includes a variable gain amplifier, where an amplifier gain is set as a function of an entire carrier multiplex present on the first number of input signals.

The disclosure of KIM would in no way lead one skilled in the art to determine that this feature is inherent in the disclosure of SMITH et al.

For at least the foregoing reasons, Applicant submits that claim 1 is not anticipated by SMITH et al. and KIM, whether taken alone or in any reasonable combination.

Claims 27 and 28 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by BEAMISH et al. Applicant respectfully traverses this rejection.

Independent claim 27 is directed to device including a variable gain amplifier coupled to an input of an analog-to-digital (A/D) converter and being configured to amplify carrier signals; and a scaler configured to receive a digital stream of data from the A/D converter and dynamically scale the digital stream of data to an essentially same peak magnitude. BEAMISH et al. does not disclose or suggest this combination of features.

For example, BEAMISH et al. does not disclose or suggest a variable gain amplifier coupled to an input of an A/D converter and being configured to amplify carrier signals. The Examiner relies on element 290 in Fig. 2 of BEAMISH et al. as allegedly corresponding to the recited variable gain amplifier (Office Action, pg. 4). Applicant respectfully disagrees with the Examiner's interpretation of BEAMISH et al.

Element 290 in Fig. 2 of BEAMISH et al. corresponds to an attenuation circuit. While attenuation circuit 290 is coupled to an input of an A/D converter 220, BEAMISH et al. does not disclose or suggest that attenuation circuit 290 is a variable gain amplifier, as recited in claim 27. In fact, BEAMISH et al. specifically discloses that attenuation circuit 290 attenuates the amplitude of an incoming signal (i.e., reduces the amplitude) from demodulator 212 (col. 5, lines 57-60). BEAMISH et al. in no way discloses or suggests that attenuation circuit 290 amplifies carrier signals (i.e., increases the amplitude), as recited in claim 27.

For at least the foregoing reasons, Applicant submits that claim 27 is not anticipated by BEAMISH et al.

Claim 28 depends from claim 27. Therefore, claim 28 is not anticipated by BEAMISH et al. for at least the reasons given above with respect to claim 27. Moreover, this claim recites an additional feature not disclosed or suggested by BEAMISH et al.

Claim 28 recites a baseband converter operatively coupled to the scaler and being configured to receive the scaled digital stream of data and digitally down-convert the scaled digital stream of data to baseband orthogonal component streams. The Examiner relies on element 240 in Fig. 2 of BEAMISH et al. as allegedly corresponding to this feature (Office Action, pg. 4). Applicant respectfully disagrees with the Examiner's interpretation of BEAMISH et al.

Element 240 in Fig. 2 of BEAMISH et al. corresponds to a receiver circuit. BEAMISH et al. discloses that receiver circuit 240 includes standard circuitry found at the back end of digital communications receivers (col. 6, lines 5-6). BEAMISH et al. in no way discloses or suggests that receiver circuit 240 includes a baseband converter that is configured to receive a scaled digital stream of data and digitally down-convert the scaled digital stream of data to baseband orthogonal component streams, as recited in claim 28. If this rejection is maintained, Applicant respectfully requests that the Examiner specifically point out where in BEAMISH et al. it is disclosed that receiver circuit 240 includes the baseband converter recited in Applicant's claim 28.

For at least these additional reasons, Applicant submits that claim 28 is not anticipated by BEAMISH et al.

Claim 29 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over BEAMISH et al. in view of O'DONNELL et al. Applicant respectfully traverses this rejection.

Claim 29 depends from claim 28. The disclosure of O'DONNELL et al. does not remedy the deficiencies in the disclosure of BEAMISH et al. set forth above with respect to claim 28. Therefore, claim 29 is patentable over BEAMISH et al. and O'DONNELL et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 28.

In view of the foregoing amendments and remarks, Applicant respectfully requests the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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